Claims

What is claimed is:

1. A method used to form a semiconductor device comprising:

providing a semiconductor wafer section comprising a bond pad having first and second portions which are electrically separated;

providing a first circuit portion electrically coupled with said first bond pad portion;

providing a second circuit portion electrically coupled with said second bond pad portion and electrically isolated from said first circuit portion; and

electrically connecting said first and second pad portions to electrically connect said first and second circuit portions.

2. The method of claim 1 further comprising attaching a ball bond to said first and second bond pad portions during said electrically connecting of said first and second pad portions.

3. The method of claim 1 further comprising attaching a wire bond to said first and second bond pad portions during said electrically connecting of said first and second pad portions.

4. The method of claim 1 further comprising screen printing a conductive epoxy to said first and second bond pad portions during said electrically connecting of said first and second pad portions.

5. The method of claim 1 further comprising:

providing a third bond pad and a third circuit portion, wherein said third pad portion is electrically coupled with said third circuit portion and is electrically isolated from said first and second circuit portions; and

during said electrically connecting said first and second pad portions, electrically connecting said first, second, and third pad portions to electrically connect said first, second, and third circuit portions.

6. The method of claim 1 further comprising:

providing a transistor during said providing of said first circuit portion and providing one of a fuse and antifuse array during said providing of said second circuit portion; and

electrically coupling said one of said fuse and antifuse array to said transistor during said electrical connection of said first and second bond pad portions.

7. The method of claim 1 further comprising:

providing a lead frame; and

subsequent to electrically connecting said first and second pad portions, attaching said wafer section to said lead frame.

8. A method used during the formation of a semiconductor device comprising:

providing first and second conductive pad portions electrically isolated from each other;

providing a transistor electrically coupled with said first conductive pad portion;

providing one of a fuse array and an antifuse array, said array electrically coupled with said second conductive pad portion;

electrically coupling said second pad portion to a voltage source;

with said second pad portion electrically coupled to said voltage source, programming said array; and

subsequent to programming said array, electrically coupling said first pad portion with said second pad portion.

9. The method of claim 8 further comprising electrically coupling said second pad portion to said voltage source through a probe tip during said electrical coupling of said second pad portion with said voltage source.

10. The method of claim 8 further comprising:

providing a CGND node during said providing of said second pad portion;

electrically coupling said CGND node to said transistor during said electrical coupling of said first pad portion with said second pad portion; and

tying said CGND node to ground through said transistor during an operational mode of said semiconductor device subsequent to programming said array.

11. A method used to form a semiconductor device comprising:

providing a semiconductor wafer substrate assembly;

providing a bond pad comprising at least three separate sections electrically isolated from each other, wherein said three sections of said bond pad each overlie said wafer substrate assembly;

providing at least three circuit portions with one circuit portion electrically connected with only one of said bond pad portions;

electrically interconnecting said at least three bond pad sections to electrically connect said at least three circuit portions.

12. The method of claim 11 further comprising:

providing a lead frame; and

subsequent to electrically interconnecting said at least three bond pad sections, attaching said semiconductor wafer substrate assembly to said lead frame.

13. The method of claim 11 further comprising attaching a ball bond to said at least three bond pad sections during said interconnection of said at least three bond pad sections.

14. The method of claim 11 further comprising screen printing a conductive material to contact said at least three bond pad sections during said interconnection of said at least three bond pad sections.

15. A method used to form a semiconductor device comprising:

providing a semiconductor wafer substrate assembly;

providing a plurality of conductive pads electrically isolated from each other;

providing a plurality of circuits wherein each circuit is electrically connected with one of said bond pads;

selecting an operational mode of said semiconductor device by selectively connecting at least two of said plurality of conductive pads to each other to selectively connect at least two of said plurality of circuits.

16. The method of claim 15 further comprising encapsulating said semiconductor wafer substrate assembly subsequent to said selection of said operational mode.

17. A method used during the formation of a semiconductor device comprising:

providing a semiconductor wafer section;

forming first and second spaced conductive pads on said semiconductor wafer section; and

forming first and second internal power buses on said semiconductor wafer section, wherein said first power bus is electrically connected to said first conductive pad and said second power bus is electrically connected to said second conductive pad,

wherein said first and second conductive pads are adapted to be electrically coupled to electrically connect said first power bus with said second power bus.

18. The method of claim 17 further comprising forming a V_{SS} power bus and a V_{SSQ} power bus during said formation of said first and second internal power buses.

19. The method of claim 17 further comprising electrically connecting said first conductive pad with said second conductive pad to electrically connect said V_{SS} power bus with said V_{SSQ} power bus.

20. A semiconductor device comprising:

a semiconductor wafer substrate assembly comprising a first circuit and a second circuit; and

a conductive pad comprising a first conductive pad portion overlying said wafer substrate assembly electrically coupled with said first circuit and a second conductive pad portion overlying said wafer substrate assembly electrically coupled with said second circuit, wherein said first and second conductive pad portions are adapted to be electrically connected to each other and to electrically connect said first circuit to said second circuit.

21. The device of claim 20 further comprising an electrically conductive interconnection adapted to electrically connect said first and second conductive pad portions to each other.

22. The device of claim 20 further comprising a ball bond which electrically connects said first and second conductive pad portions to each other.

23. The device of claim 20 wherein said device is functional only if said first and second circuits are electrically connected to each other.